

74LVT04

3.3 V Hex inverter

Rev. 4 — 12 August 2021

Product data sheet

1. General description

The 74LVT04 is a hex inverter. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

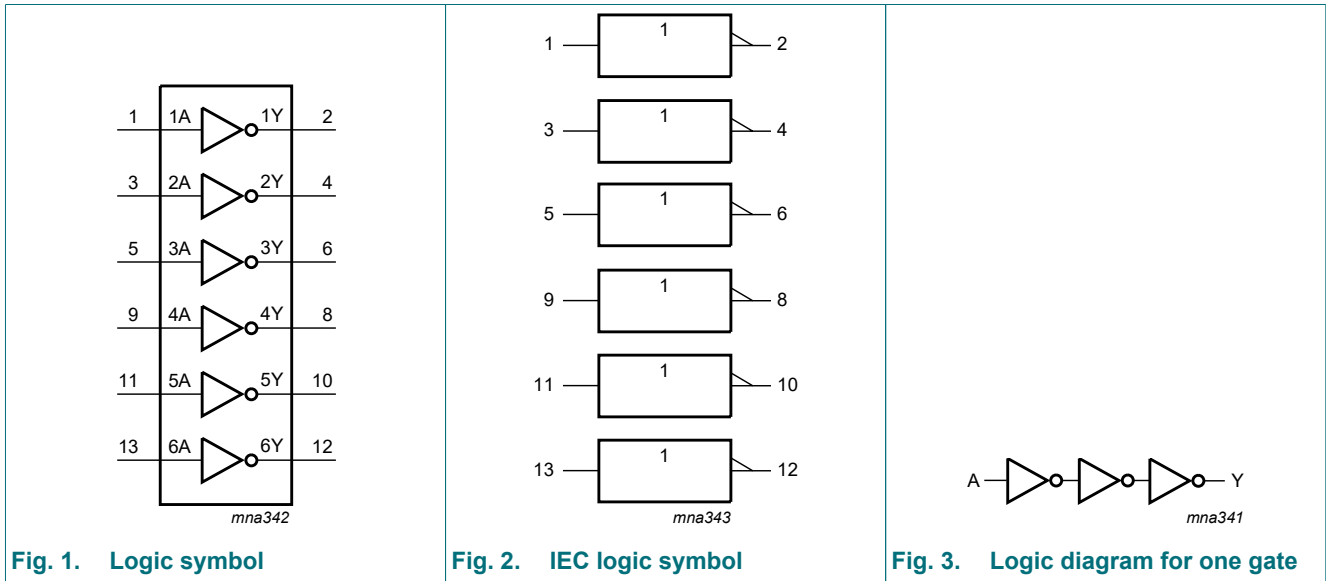
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

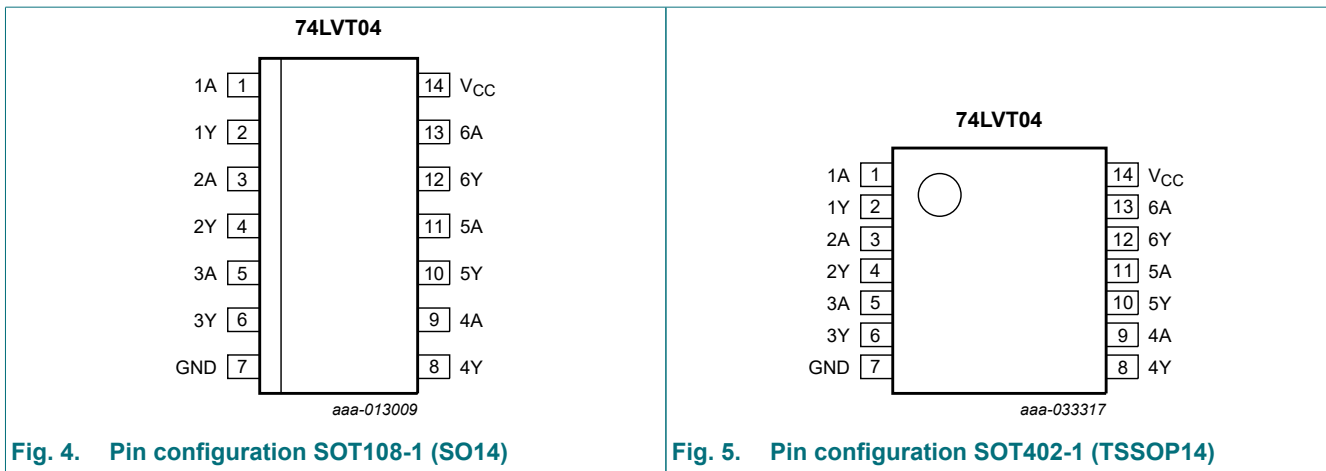
| Type number | Package | | | |
|-------------|-------------------|---------|---|----------|
| | Temperature range | Name | Description | Version |
| 74LVT04D | -40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVT04PW | -40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------------|----------------|
| nA | 1, 3, 5, 9, 11, 13 | data input |
| nY | 2, 4, 6, 8, 10, 12 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

| Input | Output |
|-------|--------|
| nA | nY |
| L | H |
| H | L |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---------------------------------------|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | [1] | -0.5 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state [1] | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 64 | mA |
| | | output in HIGH-state | - | -32 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | [2] | - | 150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +85 °C [3] | - | 500 | mW |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|-----------------|-----|-----|------|
| V_{CC} | supply voltage | | 2.7 | 3.6 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | - | -20 | mA |
| I_{OL} | LOW-level output current | | - | 32 | mA |
| T_{amb} | ambient temperature | in free air | -40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|---------------------------|---|-----------------------|---------|------|------|
| | | | Min | Typ [1] | Max | |
| V _{IK} | input clamp voltage | V _{CC} = 2.7 V; I _{IK} = -18 mA | - | - | -1.2 | V |
| V _{OH} | LOW-level input voltage | V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA | V _{CC} - 0.2 | - | - | V |
| | | V _{CC} = 2.7 V; I _{OH} = -6 mA | 2.4 | - | - | V |
| | | V _{CC} = 3.0 V; I _{OH} = -20 mA | 2.0 | - | - | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.7 V; I _{OL} = -100 μA | - | - | 0.2 | V |
| | | V _{CC} = 2.7 V; I _{OL} = 24 mA | - | - | 0.5 | V |
| | | V _{CC} = 3.0 V; I _{OL} = 32 mA | - | - | 0.5 | V |
| I _I | input leakage current | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | - | 10 | μA |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | - | ±1 | μA |
| I _{OFF} | output off current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | - | ±100 | μA |
| I _{CCH} | quiescent supply current | V _{CC} = 3.6 V; outputs HIGH; V _I = GND or V _{CC} ; I _O = 0 V | - | - | 0.02 | mA |
| I _{CCL} | quiescent supply current | V _{CC} = 3.6 V; outputs LOW; V _I = GND or V _{CC} ; I _O = 0 V | - | 1.5 | 3 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V; other inputs at V _{CC} or GND [2] | - | - | 0.2 | mA |
| C _I | input capacitance | V _I = 3 V or 0 V | - | 3 | - | pF |

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

[2] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Fig. 7.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|------------------------------------|---------------------------------|------------------|---------|-----|------|
| | | | Min | Typ [1] | Max | |
| t _{PLH} | LOW to OFF-state propagation delay | nA to nY; see Fig. 6 | | | | |
| | | V _{CC} = 2.7 V | - | - | 4.7 | ns |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.0 | 2.6 | 3.9 | ns |
| t _{PHL} | OFF-state to LOW propagation delay | nA to nY; see Fig. 6 | | | | ns |
| | | V _{CC} = 2.7 V | - | - | 3.2 | |
| | | V _{CC} = 3.3 V ± 0.3 V | 1.0 | 2.5 | 3.5 | ns |

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

10.1. Waveform and test circuit

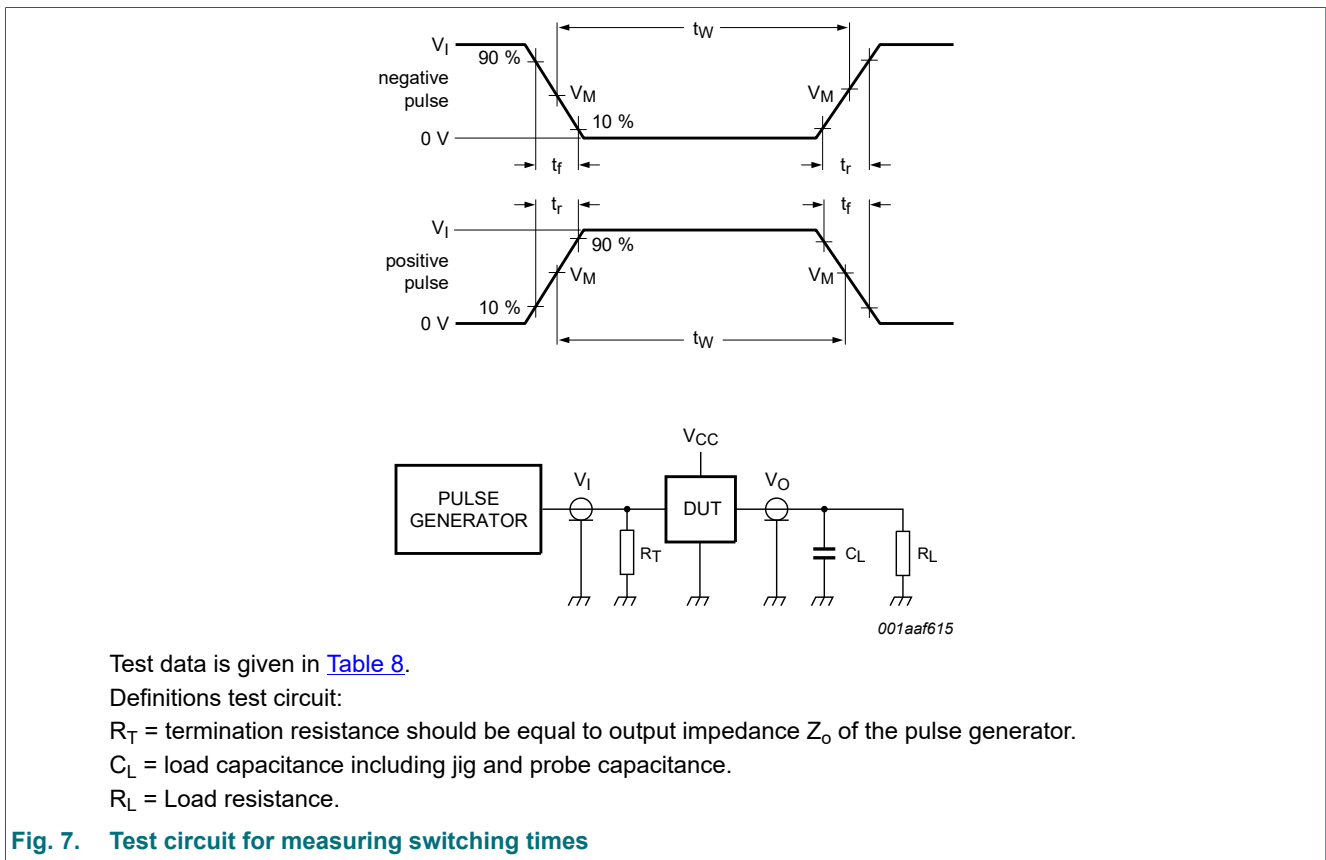
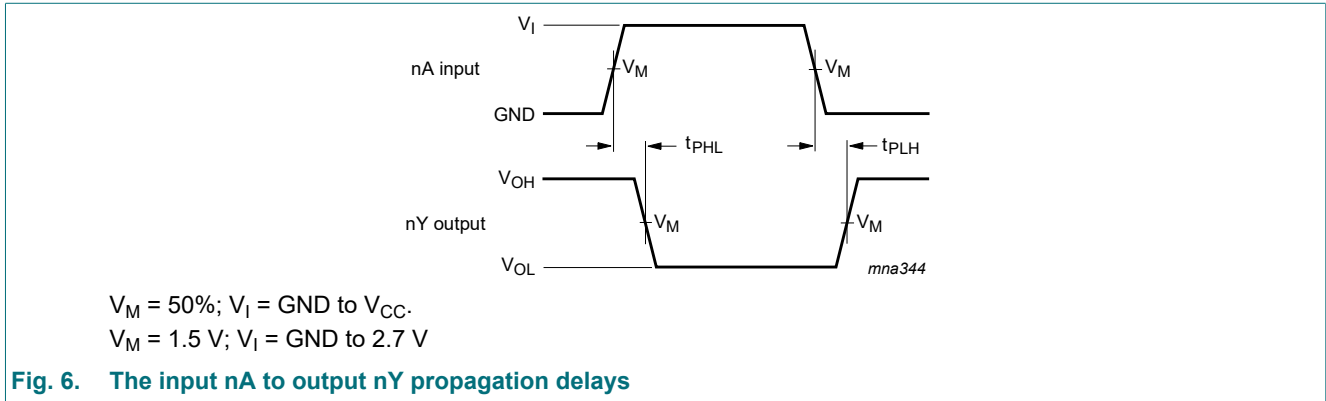


Table 8. Test data

| Input | | | | Load | |
|-------|-----------------------|--------|-----------------------|-------|--------------|
| V_I | f_i | t_W | t_r, t_f | C_L | R_L |
| 2.7 V | $\leq 10 \text{ MHz}$ | 500 ns | $\leq 2.5 \text{ ns}$ | 50 pF | 500 Ω |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

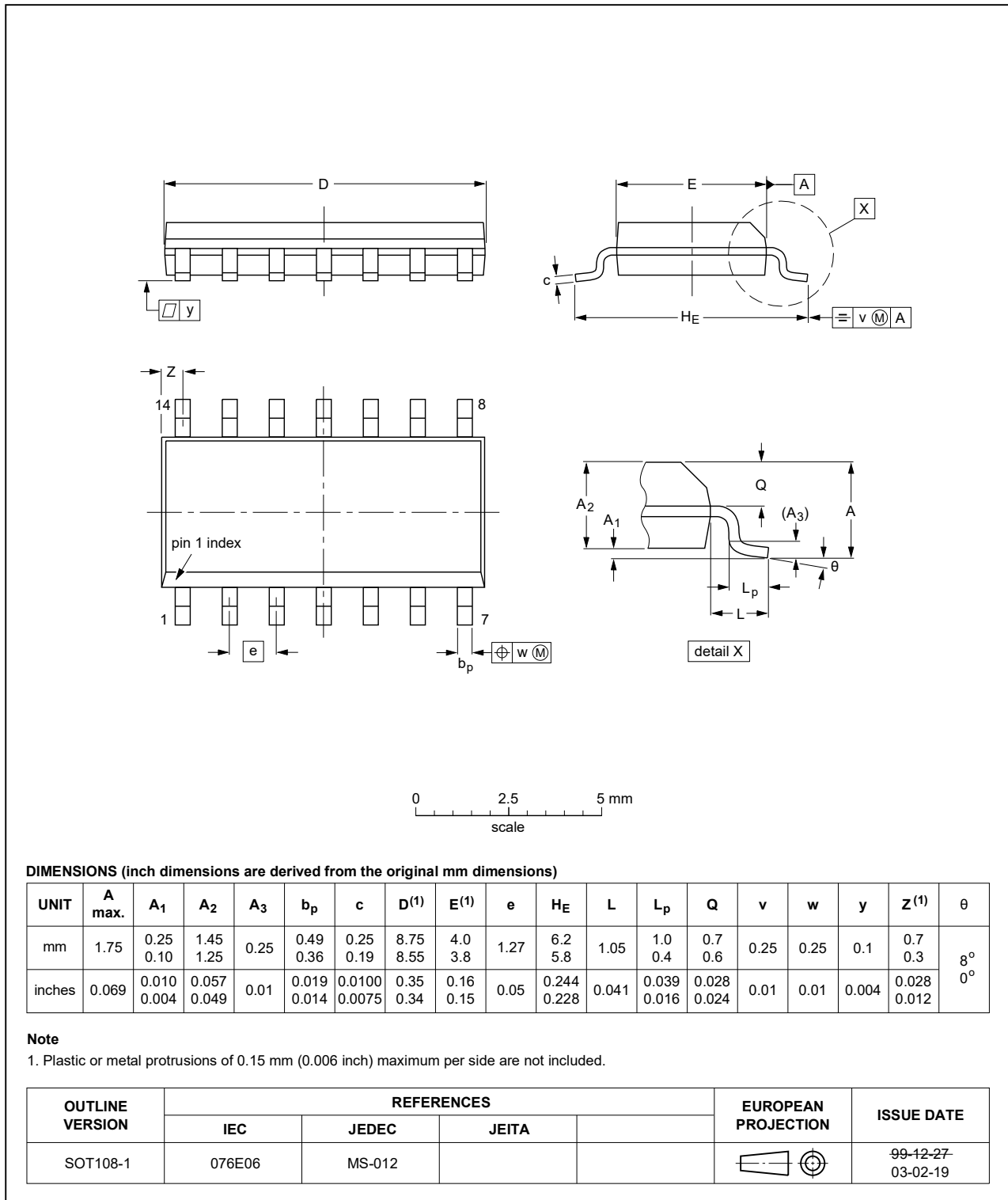


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

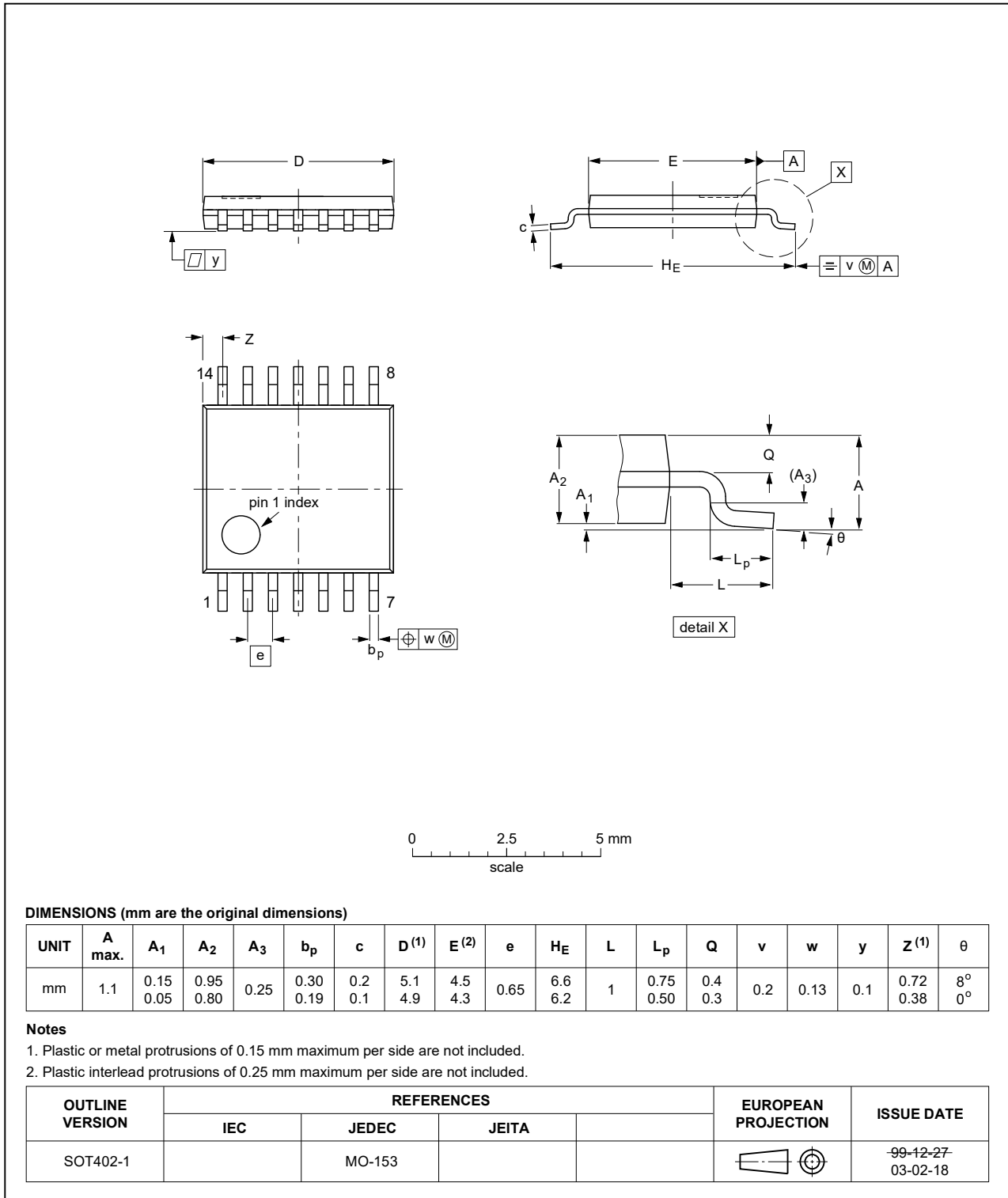


Fig. 9. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|-------------|
| 74LVT04 v.4 | 20210812 | Product data sheet | - | 74LVT04 v.3 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LVT04DB (SOT337-1/SSOP14) removed. | | | |
| 74LVT04 v.3 | 20210401 | Product data sheet | - | 74LVT04 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated. Section 9: Unit of ΔI_{CC} corrected to mA (Errata). | | | |
| 74LVT04 v.2 | 20140428 | Product data sheet | - | 74LVT04_1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Imported the data sheet into the latest template | | | |
| 74LVT04_1 | 19960828 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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